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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/541,076	06/29/2005	Dennis Ciplickas	524322000200	4078
20872	7590	07/17/2008	EXAMINER	
MORRISON & FOERSTER LLP 425 MARKET STREET SAN FRANCISCO, CA 94105-2482				SIEK, VUTHE
ART UNIT		PAPER NUMBER		
		2825		
		MAIL DATE		DELIVERY MODE
		07/17/2008		PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/541,076	CIPLICKAS ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 16 April 2008.
- 2a) This action is **FINAL**.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-67 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1,34,37 and 67 is/are rejected.
- 7) Claim(s) 2-33,35,36 and 38-66 is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:
1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ .                                    |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ .  | 6) <input type="checkbox"/> Other: _____ .                        |

## DETAILED ACTION

1. This office action is in response to application 10/541,076 and amendment filed on 04/16/2008. Claims 1-67 remain pending in the application.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 34, 37 and 67 are rejected under 35 U.S.C. 102(e) as being anticipated by Stine et al. (6,901,564 B2).

4. As to claims 1, 37 and 67, Stine et al. teach substantial the same the claim limitations of designing an IC to improve yield comprising obtaining a design element (Fig. 19); creating a variant design element by modifying a feature (Fig. 18; layout attributes; col. 4 lines 18-31; col. 5; col. 7); determining a yield to area ratio and if the yield to area ratio is greater than a yield to area ratio of the obtained design element retaining the variant design element to be used in designing the IC (col. 13-14). In addition, Stine et al. teach the predictable product yield obtained can be that associated with each defined attribute, functional block, or layer, or the resultant yield prediction for the entire product

layout. For example, the product layout is analyzed to determine line space distribution, width distribution, density distribution, the number of island patterns, in effect developing a subset of the entire set of design rules of the fabrication process (col. 5 lines 9-51).

5. As to claim 34, Stine et al. the yield improvement of the layout modification as taught by Stine would impliedly include determine post-layout modifications to improve yield and reliability and manufacturing process.

***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1, 34, 37 and 67 are rejected under 35 U.S.C. 103(a) as being obvious over Allan, "Yield/Reliability Enhancement using Automated Minor Layout Modifications," IEEE, 2000, pages 252-261 in view of Satya et al., (6,751,519 B1).

8. As to claims 1, 37 and 67, Allan teaches obtaining a design element of an integrated circuit design and creating a design layout modification for a selected design element (a variant design element) by modifying a feature of the design element to improve yield/reliability (see whole document). Allan does not teach determining a yield to area ratio and if the determined yield to area ratio is greater than a yield to area ratio of the obtained design element, retaining the variant design element to be used in

designing the integrated circuit. Satya et al. appears to teach yield information that includes systematic yield component  $Y_o$  which is independent of area (col. 6, lines 38-67; col. 7 lines 1-60). In addition, Satya et al. appears to teach the area in the yield to area ratio corresponds to the area of the entire variant design element (Fig. 5A). the figure shows a ratio of the narrow area 509 and the area of the window 500 (entire variant design element) is the probability of fail for defect 508 having a size about equal to the spacing 506 (col. 7 lines 49-53). This suggests that any improvement of  $Y_o$  (when a yield to area ratio due to the change is greater than a yield to area ration of the obtained design element) is would keep any changes to the design elements (variant design element) to be used in designing the integrated circuit. With that suggestion, it would have been obvious to practitioners in the art at the time the invention was made to determine a yield to area ratio and if the determined yield to area ratio is greater than a yield to area ratio of the obtained design element, retaining the variant design element to be used in designing the integrated circuit because this would improve yield and reliability of the circuit design.

9. As to claim 34, Allan and Satya et al. do not teach post-layout tape-out modifications. However, post-layout tape-out modifications is known in the art is well known in the art. Utilizing this well known art limitation would be obvious to one of ordinary skill in the art at the time the invention was made because any minor modification to layout would improve manufacturing of the semiconductor product.

***Allowable Subject Matter***

10. Claims 2-9; 10-12; 13-33; 26; 35-36; 38-64 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Remarks***

11. Applicants argued that the reference do not the area in the yield to area ratio corresponds to the area of the entire variant design element. Examiner disagreed. The above rejection clarifies Examiner's position. Applicants do not clearly explain the claim limitation and specifically point out where the specification describes those limitations.

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Vuthe Siek/  
Primary Examiner, A.U. 2825